What is claimed is:

1. A circuit for spread spectrum clock generation, comprising:

a phase detection circuit that is configured to provide an error signal from a reference signal and a feedback signal;

a voltage controlled oscillator circuit that is configured to provide a synthesized signal from the error signal;

a modulating waveform generator circuit that is configured to provide a modulating waveform signal that varies over time as a modulating waveform;

an accumulator circuit that is configured to provide a carry signal from the modulating waveform signal; and

an adjustable clock divider circuit that is configured to provide an adjustable clock divider output signal from an adjustable clock divider input signal, wherein the adjustable clock divider input signal is based at least in part on the synthesized signal, the feedback signal is based at least in part on the adjustable clock divider output signal, and wherein the adjustable clock divider circuit is configured to provide the adjustable clock divider output signal such that a frequency that is associated with the adjustable clock divider signal corresponds to the frequency associated with the adjustable clock divider input signal divided by:

a first number, if the carry signal is associated with a first logic level, and

a second number, if the carry signal is associated with a second logic level.

2. The circuit of Claim 1, wherein the second number equals the first number minus one.

3. The circuit of Claim 1, wherein the modulating waveform is suitable for reducing electromagnetic interference.

4. The circuit of Claim 1, wherein the modulating waveform includes one of a triangle wave and a sinusoidal wave.

5. The circuit of Claim 1, wherein the accumulator circuit includes a digital adder circuit having first and second inputs, a sum output, and a carry output, wherein the digital adder circuit is arranged to receive the modulated waveform signal at the first input, the sum output is coupled to the second input, and wherein the digital adder circuit is configured to provide the carry signal at the carry output.

6. The circuit of Claim 1, wherein the phase detection circuit includes a phase detector, a charge pump circuit, and a low-pass filter circuit.

7. The circuit of Claim 1, further comprising a clock divider circuit that is configured to provide the adjustable clock divider input signal from the synthesized signal.

8. The circuit of Claim 1, wherein the modulating waveform signal includes a multiple-bit digital word that varies over time according to the modulating waveform.

9. The circuit of Claim 1, further comprising:

a clock divider circuit that is configured to provide an output clock signal from the synthesized signal.

10. The circuit of Claim 9, wherein the clock divider circuit is configured to provide the output signal such that a frequency that is associated with the output clock signal corresponds to a frequency that is associated with the synthesized signal divided by a third number.

11. The circuit of Claim 1, wherein the modulating waveform is suitable for spreading a frequency spectrum that is associated with the synthesized signal relative to a

frequency spectrum that is associated with the reference signal according to a down-spread modulation.

12. The circuit of Claim 11, wherein the down-spread modulation is between approximately -.5% to -1.5%.

13. A circuit for spread spectrum clock generation, comprising:

a phase detection circuit that is configured to provide an error signal from a phase detection input signal and a feedback signal;

a voltage controlled oscillator circuit that is configured to provide a synthesized signal from the error signal, wherein the feedback signal is based at least in part on the synthesized signal;

a modulating waveform generator circuit that is configured to provide a modulating waveform signal that varies over time as a modulating waveform;

an accumulator circuit that is configured to provide a carry signal from the modulating waveform signal; and

an adjustable clock divider circuit that is configured to provide an adjustable clock divider output signal from an adjustable clock divider input signal, wherein the adjustable clock divider input signal is based at least in part on a reference signal, the phase detection input signal is based at least in part on the adjustable clock divider output signal, and wherein the adjustable clock divider circuit is configured to provide the adjustable clock divider output signal such that a frequency that is associated with the adjustable clock divider signal corresponds to the frequency associated with the adjustable clock divider input signal divided by:

a first number, if the carry signal is associated with a first logic level, and

a second number, if the carry signal is associated with a second logic level.

14. The circuit of Claim 13, further comprising a clock divider circuit that is configured to provide the feedback signal from the synthesized signal.

15. The circuit of Claim 13, wherein the second number equals the first number minus one.

16. The circuit of Claim 13, wherein the modulating waveform includes at least one of a triangle wave and a sinusoidal wave.

17. The circuit of Claim 13, wherein the modulating waveform signal includes a multiple-bit digital word that varies over time according to the modulating waveform.

18. The circuit of Claim 13 further comprising:

a clock divider circuit that is configured to provide an output signal from the synthesized signal.

19. The circuit of Claim 18, wherein the clock divider circuit is configured to provide the output signal such that a frequency that is associated with the output signal corresponds to a frequency that is associated with the synthesized signal divided by a third number.

20. A circuit for spread spectrum clock generation, comprising:

means for determining a phase difference between a reference signal and a feedback signal;

means for providing a synthesized signal from the determined phase difference;

means for providing modulating waveform signal that includes a multiple-bit digital word that varies over time as a modulating waveform;

means for providing a carry signal from the modulating waveform signal such that a frequency of pulses in a logical level that is associated with the carry signal is determined according to a value that is associated with the multiple-bit digital word;

means for frequency division by a first number if the carry signal is associated with a first logic level; and

means for frequency division by a second number if the carry signal is associated with a second logic level.